DJJ-003-015406 Seat No. _____

# M. Sc. (Electronics) (Sem. IV) (CBCS) Examination

**May / June – 2015**

## Paper - 16 : Designing Hardware with Software using VHDL.

**Faculty Code : 003**
**Subject Code : 015406**

Time : $2\frac{1}{2}$ Hours] [Total Marks : **70**

**Q1. Answer the Following in brief (Any seven out of ten, Each carry 2 marks) ...(14)**

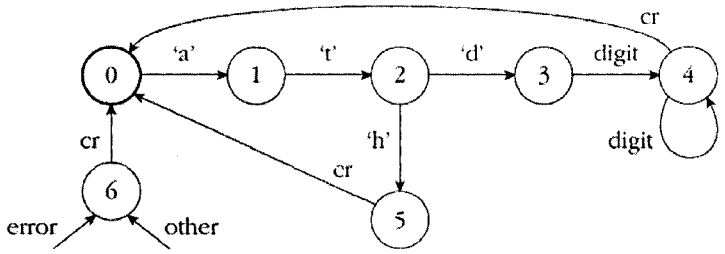
1. What is sensitivity list in process block? Is there any alternative to sensitivity list.
2. Write the difference between transport and inertial delay with suitable example.
3. Explain simulator and synthesizer in brief.
4. What is unconstrained array? Explain with suitable example.
5. What is VHDL? How it is differ from traditional programming language?
6. What is generic? Explain in brief.
7. Write the difference between verification and testing in context of digital circuit development process.
8. Explain report statement in brief.
9. Explain entity and architecture in context of VHDL with suitable example.
10. Consider the following VHDL program

```
library ieee;
use ieee. std-logic-1164. all ;

entity and_gate is
      port (
            a, b: in std-logic;
            x , y: out std-logic
           ) ;
end and_gate ;

architecture arch of and_gate is
begin
     x <= a and b;
     y <= not x ;
end arch ;
```

Find error if any. If there is an error, write the method to solve it.

**2.Answer the Following(Any 2 out of 3, each carry 7 marks)** **...(14)**

1. The state transition diagram for a modem command finite-state machine is shown in following figure. State 0 is the initial state. The machine returns to this state after recognizing a correct command. State 6 is the error state, to which the machine goes if it detects an illegal or unexpected character. Write a VHDL module to construct FSM to select state according to input command, no need to explain processing of the command.




2. Write a note on "simulation deltas".
3. Explain the internal architecture of CPLD and FPGA in detail. Also give example of 3-input XOR gate design for FPGA.

**3.Answer the following (each carry 7 marks)** **...(14)**

1. Write a short note on verification. Also explain various method of verification.
2. Write the VHDL model to create "4 to 2 priority encoder" using selective signal assignment and conditional signal assignment with suitable circuit diagram and truth table.

**OR**

**3.Answer the following (each carry 7 marks)** **...(14)**

1. Write a short note on "domain and level of modeling of system".
2. Write the VHDL model to create "2 to 4 decoder" using sequential if...else and case statement with suitable circuit diagram and truth table.

**4.Answer the following (Each carry 7 marks).** **...(14)**

1. Write the structural and behavioral model of VHDL to create "3-bit even parity detector" with suitable circuit diagram and truth table.
2. What is driver in context of VHDL? How can we resolve the bad driver situation in synthesis, explain it with suitable 4 to 1 multiplexer example.

**5.Answer the following (Any 2 out of 4, each carry 7 marks).** **...(14)**

1. Write a note on "Lexical elements of VHDL".
2. Design VHDL behavior model to create modulo 16 counter with reset condition.
3. Explain data types Boolean, Bit, std_ulogic and their vector.
4. Write various methods to detect clock's edges and explain each of them in brief.